

WHAT IS CLAIMED IS:

1 1. A method for aligning an input clock signal with a delay clock signal,
2 the method comprising:
3 detecting phases of the input clock signal and the delay clock signal to
4 generate a phase detection signal;
5 detecting edges of the delay clock signal to generate a detect signal;
6 selecting the delay clock signal or the input clock signal to provide a selection
7 signal in response to the detect signal; and
8 controlling a delay of the selection signal in response to the phase detection
9 signal to generate the delay clock signal.

1 2. The method of claim 1 wherein detecting the phases of the input clock
2 signal and the delay clock signal further comprises:
3 dividing a frequency of the delay clock signal using a first frequency divider
4 to generate a first frequency divided delay signal; and
5 comparing phases of the input clock signal with the first frequency divided
6 delay signal to generate the phase detection signal using a phase comparator.

1 3. The method of claim 2 further comprising:
2 dividing the frequency of the delay clock signal using a second frequency
3 divider to generate an output clock signal.

1 4. The method of claim 3 further comprising:
2 providing the output clock signal to programmable circuit elements in a
3 programmable integrated circuit.

1 5. The method of claim 1 wherein selecting the delay clock signal or the
2 input clock signal to provide the selection signal in response to the detect signal further
3 comprises:
4 coupling a feedback loop around an adjustable delay circuit to form an
5 oscillator circuit that generates the delay clock signal when the detect signal has a first value
6 that selects the delay clock signal as the selection signal; and
7 decoupling the feedback loop from an input of the adjustable delay circuit
8 when the detect signal has a second value that selects the input clock signal as the selection
9 signal.

1 6. The method of claim 1 wherein controlling the delay of the selection
2 signal in response to the phase detection signal to generate the delay clock signal further
3 comprises:
4 increasing the delay of the selection signal through an adjustable delay circuit
5 when the phase detection signal indicates that an edge of the delay signal is ahead of a
6 corresponding edge of the input signal; and
7 decreasing the delay of the selection signal through the adjustable delay circuit
8 when the phase detection signal indicates that an edge of the delay signal is behind a
9 corresponding edge of the input signal.

1 7. The method of claim 1 wherein selecting the delay clock signal or the
2 input clock signal to provide the selection signal in response to the detect signal further
3 comprises:
4 selecting the delay clock signal as the selection signal regardless of the value
5 of the detect signal when a disable signal has a predefined value.

1 8. A circuit for aligning a periodic input signal with a delay signal, the
2 circuit comprising:
3 a phase detector having a first input coupled to the periodic input signal;
4 an adjustable delay circuit coupled to an output of the phase detector that
5 generates the delay signal at an output of the adjustable delay circuit;
6 a feedback loop circuit coupled to the output of the adjustable delay circuit;
7 an edge detector circuit having an input coupled to the output of the adjustable
8 delay circuit; and
9 a multiplexer having data inputs coupled to the feedback loop and the periodic
10 input signal, a select input coupled to receive a detect signal from the edge detector circuit,
11 and an output coupled to an input of the adjustable delay circuit.

1 9. The circuit according to claim 8 further comprising:
2 a first frequency divider circuit having an input coupled to the output of the
3 adjustable delay circuit and an output coupled to a second input of the phase detector, the first
4 frequency divider dividing a frequency of the delay signal by N to generate a divided signal.

1 10. The circuit according to claim 9 wherein the edge detector circuit
2 generates a HIGH pulse one-half a period of the delay signal before a rising edge of the
3 divided signal.

1 11. The circuit according to claim 9 wherein the first frequency divider is a
2 counter circuit, and the edge detector circuit generates a HIGH pulse after the counter circuit
3 counts a predetermined number of edges of the delay signal.

1 12. The circuit according to claim 9 further comprising:
2 a second frequency divider circuit having an input coupled to the output of the
3 adjustable delay circuit that generates a periodic output signal, wherein the second frequency
4 divider divides a frequency of the delay clock signal by M, and the periodic output signal has
5 a frequency that is N/M times the frequency of the input signal.

1 13. The circuit according to claim 8 further comprising:
2 a logic gate coupled to the select input of the multiplexer, to an output of the
3 edge detector circuit, and to a memory cell.

1 14. The circuit according to claim 8 wherein the adjustable delay circuit
2 comprises an odd number of inverting buffers coupled together in series.

1 15. The circuit according to claim 8 wherein:
2 the feedback loop is coupled to the input of the adjustable delay circuit when
3 the detect signal is in a first state, and the input of the adjustable delay circuit receives the
4 periodic input signal when the detect signal is in a second state,
5 the edge-detector circuit causing the detect signal to transition from the first
6 state to the second state, and causing the detect signal to transition from the second state to
7 the first state after one period of the delay signal.

1 16. A circuit for aligning an input clock signal with a delay signal, the
2 circuit comprising:
3 means for detecting a phase difference between the input clock signal and the
4 delay signal to generate a phase difference signal;
5 means for controlling a phase of the delay signal in response to the phase
6 difference signal;

7 means for detecting edges of the delay signal to generate a detect signal; and
8 means for selecting the input clock signal or the delay signal as a selected
9 signal in response to a value of the detect signal, wherein the selected signal is delayed by the
10 means for controlling to generate the delay signal.

1 17. The circuit defined in claim 16 further comprising:
2 means for dividing a frequency of the delay signal by N to generate a first
3 divided signal, wherein the means for detecting the phase difference between the input clock
4 signal and the delay signal compares the input clock signal to the first divided signal.

1 18. The circuit defined in claim 17 further comprising:
2 means for dividing the frequency of the delay signal by M to generate an
3 output clock signal, wherein a frequency of the output clock signal is N/M times the
4 frequency of the input clock signal.

1 19. The circuit defined in claim 16 further comprising:
2 means for causing the means for selecting to select the delay signal as the
3 selected signal regardless of the value of the detect signal when a disable signal is a
4 predetermined value.

1 20. The circuit defined in claim 16 wherein the means for detecting the
2 edges of the delay signal counts falling edges of the delay signal.

1 21. The circuit defined in claim 16 wherein the means for selecting selects
2 the delay clock signal as the selected signal during a first state of operation, and the means for
3 selecting selects the input clock signal as the selected signal for one period of the delay signal
4 during a second state of operation.

1 22. The circuit defined in claim 16 wherein the circuit for aligning the
2 input clock signal with the delay signal in part of a field programmable gate array.